Comparative Design of CMOS Class-D Audio Amplifier for Switching and Conduction Losses Operation

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***Abstract*—Recent advances related to the Internet of Things have led to the dissemination of mobile or embedded devices, many of which have audio output in the human-machine interface. Thus, class-D audio amplifiers emerged as the main alternative to switched amplifiers, given their high efficiency. In this work, we design a Class-D audio amplifier and perform a comparison between output stages optimized for switching losses and conduction losses. The proposed circuit employs pulse-width modulation (PWM) and a half-bridge configuration of the output stage. The simulation results show an average efficiency of 74.8% in the stage optimized for switching losses and 89.1% in the stage optimized for conduction losses.**

***Index Terms*—Class-D audio amplifier, PWM modulation, half-bridge output stage**

I. Introduction

In a conventional transistor amplifier, the output stage transistors operate in their linear region, which implies non-zero drain-to-source current and voltage drop in at least one output transistor, producing significant $V_{DS} \times I_{DS}$ power dissipation [1]. The overall efficiency depends on the method used to bias the output transistors, which classifies linear amplifiers into classes A, B, and AB.

In a Class-D amplifier, the output transistors operate as on-and-off switches, while off the drain-to-source current is zero, and while on the voltage drop across the transistor is negligible [2]. Thus, the Class-D amplifier has a theoretical efficiency of 100%, nonetheless, the power losses due to its implementation will limit the maximum efficiency.

High efficiency is especially crucial in high power and mobile applications. Either because of the battery life and low thermal dissipation or because of the reduction in the size of the heatsinks, which results in less volume and weight.

Several works can be found in the literature about Class-D amplifiers implemented in CMOS technology [3] and [4]. This work presents a review of the Class-D amplifier, detailing the stages and design decisions considering two distinct operating regions, in which one predominates switching losses and the other conduction losses. The amplifier was designed using a commercial 0.35 μm CMOS technology and performance parameters were investigated.

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II. Circuit Blocks

In this work, for simplicity, we consider the basic circuit of the Class-D amplifier, presented in Fig. 1, which corresponds to the half-bridge circuit and the electromagnetic speaker load is modeled as an 8 Ω resistor. The full-bridge circuit is widely used in commercial Class-D amplifiers, as it doubles the power supplied to the load. The main trade-off is the increased area, which in the case of the BD switching scheme implies duplicating the building blocks of the amplifier circuit.

A. Modulator

The PWM modulator encodes the audio signal's amplitude in the pulse widths of a square wave based on the comparison between the carrier and a sampled version of the signal. The carrier is a triangular wave that can be generated by a circuit like the one in Fig. 2, for example [5].

On the frequency domain, the modulator outputs contain the input signal component, distortion components of the input signal and a high frequency spectrum composed of the carrier frequency and noise [6].

The modulation scheme chosen is the Natural sampled - AD switching - Double sided modulation (NADD). The equation 1 shows the double Fourier series for NADD. It is evident that in natural sampling, with the appropriate filtering, the modulation process can be considered ideal in terms of distortion (no direct harmonics), allowing an exact replica of the input signal to be reconstructed [6].

$$\begin{aligned} F_{NADD}(t) =& M\cos y \\ &+ 2\sum_{m=1}^{\infty} \frac{J_0(m\pi\frac{M}{2})}{m\pi/2}\sin(\frac{m\pi}{2})\cdot\cos(mx) \\ &+ 2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty} \frac{J_n(m\pi\frac{M}{2})}{m\pi/2}\sin(\frac{(m+n)\pi}{2}) \\ &\cdot\cos(mx+ny) \end{aligned} \tag{1}$$

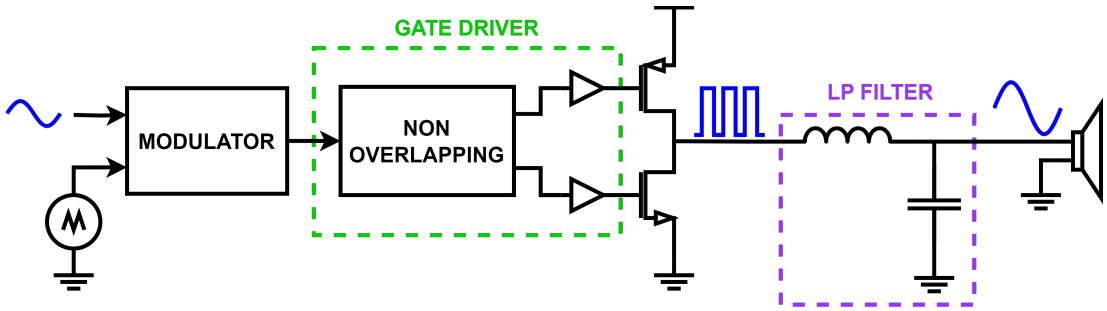

Fig. 1. Block diagram of a simplified Class-D amplifier.

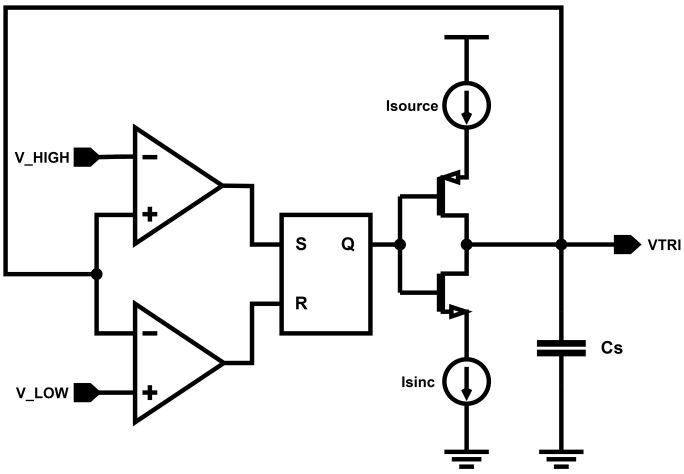

Fig. 2. Triangle wave generator schematic

The half-bridge amplifier configuration requires the AD switching method, which produce two-level modulation. This switching scheme is conceptually simple, with the output square-wave switching between the positive power supply and ground [2].

The double-sided modulation is achieved using a triangle as a reference, which gives two samples per switch period. This modulation of both edges doubles the information stored in the resulting pulse train. In this way, the effective sampling frequency is doubled although the switching frequency (and therefore the switching losses) remains the same [2].

B. Drivers

The output of the modulator consists of a low-power digital signal whose pulse width encodes the original input signal. The output stage, in turn, consists of large transistors in digital inverter configuration, sized to conduct the output current.

To drive these transistors, the modulator output signal must be conditioned to charge and discharge the capacitances of the output stage. Thus, the gate driver block consists of a non-overlapping circuit and a chain of digital inverters.

The non-overlapping circuit shown in Fig. 3, prevents the output transistors from conducting at the same time during switching, significantly reducing short-circuit current [5]. As for the cascaded digital inverters, each one with a higher W/L value, they provide the necessary current gain so that the modulated signal can drive the output stage transistors.

C. Output Stage

The power losses in a Class-D amplifier are predominated by the amplifier's quiescent power (P_Q), conduction losses (P_{CL}), switching losses (P_{SW}) and body-diode losses (P_{BD}) of the output stage [5].

The quiescent power consists of the power required by the PWM modulator and the gate driver circuit. The body-diode losses come from the body-diode conduction and its reverse recovery charge [5].

Compared to conduction and switching losses, P_Q and P_{BD} do not dominate the total amplifier losses in any region of operation. Because of this, this work will focus on the first two, P_{SW} and P_{CL}.

Conduction losses refer to the ohmic losses over the drain-source resistance (R_{ds}) of the power transistors due to in-series output current ($I_{o,RMS}$). As shown in equation 2, R_{ds} can be written as a function of the electrical permeability (μ_n), the oxide capacitance (C_{ox}), the transistor dimensions (W/L) and the overdrive voltage (v_{ov}).

$$P_{CL} = R_{ds} \cdot I_{o,RMS}^2 = \frac{I_{o,RMS}^2}{\mu_n C_{ox} \frac{W}{L} v_{ov}} \tag{2}$$

Switching losses occur due to the charging and discharging of parasitic capacitances during the transition between on and off states. The P_{SW} can be expressed as equation 3, where F_{SW} is the switching frequency, $C_{P,i}$ are the parasitic capacitors in the output stage, V_{CP} is the voltage across each parasitic capacitance, V_{DD} is the supply voltage, $\widehat{I_o}$ is the peak

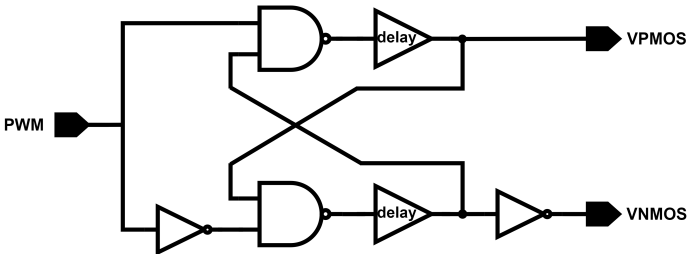

Fig. 3. Non-overlapping clocking generator

output current and t_{trans} is the transition time between ON to OFF states.

$$P_{SW} \cong \sum_i (\cdot V_{CP}^2 \cdot C_{P,i}) + 2\dot{V}_{DD} \cdot \widehat{I_o} \cdot F_{SW} \cdot t_{trans} \quad (3)$$

To minimize the P_{CL} we need to maximize the W/L parameter, as shown in equation 2 [7], which results in greater area consumption and increased parasitic capacitances. On the other hand, to minimize the P_{SW}, according to equation 3 [5], we must reduce the switching frequency and the parasitic capacitances, which implies minimizing the dimensions of the output transistors.

In low-power applications, losses are dominated by switching losses, since switching frequency and parasitic capacitances are defined by constructive aspects of the amplifier. On the other hand, in high-power applications, conduction losses are predominant due to the consequent increase in output current.

The sizing of the output transistors depends on the operation region they are intended to work and the required efficiency. As said, this work addresses two designs for the output state, one optimized to minimize switching losses and another to minimize conduction losses, both using 0.35 μm CMOS technology.

1) Switching Losses: The design of the power stage, aiming to minimize the switching losses, consists of sizing the output transistors in order to obtain the lowest W/L ratio considering the output current values. For this, we calculate the maximum output current that the amplifier is capable of supplying, which depends only on the output voltage and the type of load, as shown in Equation 4. We plot NMOS and PMOS transistor width versus gate capacitance and output current. Thus, we choose the NMOS and PMOS transistor width to drive the maximum output current and check if the gate capacitance is at acceptable levels to minimize P_{SW}.

$$I_{o,max} = \frac{V_{out,max}}{R_{load}} \quad (4)$$

2) Conduction Losses: The design of the output stage, with the objective of minimizing conduction losses, is carried out by sizing the output transistors in order to obtain the R_{ds} value that results in the desired efficiency. We estimate the value of R_{ds} as a function of the efficiency targeted by Equation 5 [5]. Then, we plot the NMOS and PMOS transistor width versus R_{ds} and output current. Thus, we choose the NMOS and PMOS transistor width that results in the desired drain-to-source resistance and verify that the transistors can conduct the maximum output current.

$$R_{ds} = \frac{R_{load}(1-\eta)}{\eta} \quad (5)$$

D. Output Low-Pass Filter

The function of the output filter is to eliminate the high frequency components related to the carrier switching frequency and coupled noise, as described in equation 1, recovering the low frequency audio signal from the modulated output.

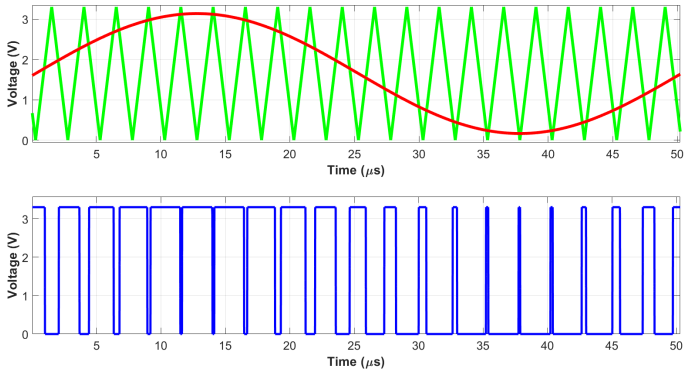

Fig. 4. Waveforms on PWM modulation

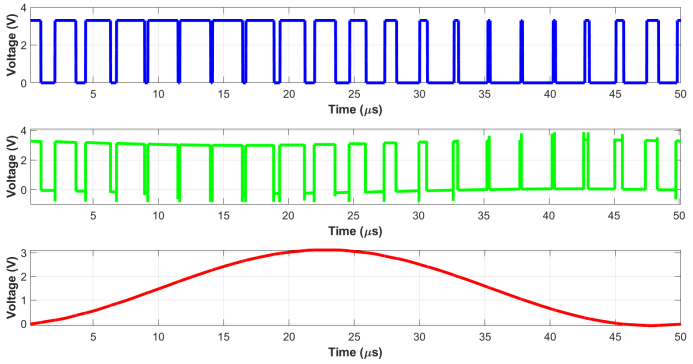

Fig. 5. Output Waveforms

An off-chip second-order low-pass filter is typically used [5]. For this implementation, the filter was designed to give a flat magnitude and linear phase response, considering a cutoff frequency of 22.5 kHz and a load of 8 Ω, the chosen inductor is 50 μH and the capacitor is 1 μF.

III. Simulation

For the following simulations, Cadence Virtuoso software was used.

A. Modulation

As illustrated in Fig. 4, PWM modulation is performed by comparing the low-frequency input signal (in red) to the high-frequency triangular carrier (green dashed line). The result is a digital output (in blue) in which the pulses' width encodes the original signal's amplitude.

B. Output Waveforms

Fig. 5 shows the main waveforms at the output of the circuit blocks that make up the amplifier. At the modulator output, we observe the PWM modulated signal in blue varying between 0V and V_{DD}. After the output stage, we obtain the signal in green composed of a low frequency fundamental, which is the replica of the input signal, and a high frequency component related to the carrier frequency. After the low pass filter, the high frequency noise is eliminated leaving only the replica of the original audio signal, shown in red, across the speaker.

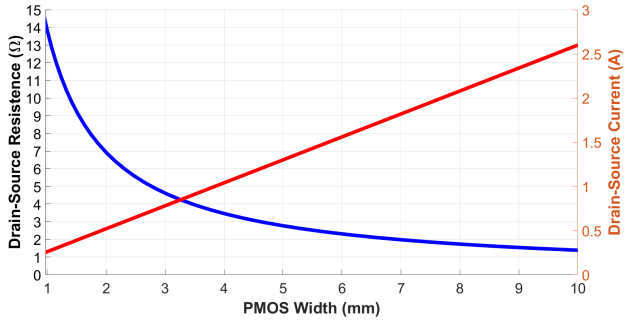

Fig. 6. PMOS transistor width versus R_{ds} and I_{ds}

C. Output stage design

The design of the output stage is based on the curves in Fig. 6, as described in section II-C. We observe that the drain-source resistance (in blue) decreases rapidly with increasing transistor width (W), but presents an asymptotic behavior for small resistance values. The drain-source current (in red) increases linearly with W.

D. comparative

Table I presents the performance parameters obtained for the two designed output stages. For a fair comparison, we only take into account the operating region for which the output stage has been optimized. The operating regions were defined in II-C according to the output power levels of the amplifier.

To compare output stages with very different power ranges, we normalize the output power in relation to the maximum output power of the amplifier, obtaining the relative power that varies from 0 to 1. Subsequently, the range of output powers was subdivided into low-power levels as less than 0.3, medium-power levels from 0.3 to 0.7 and high-power levels above 0.7 [5].

Analyzing the table I, the discrepancy in area consumption between both stages is remarkable. What was already expected since the reduction of the drain-source resistance of the output transistors implies a larger area, while reducing the output stage capacitances leads to minimizing the circuit area, as discussed in subsection II-C.

Similarly, the average output power of both stages differed greatly, given the different operating regions considered. It is noteworthy that in the full bridge configuration, the output power is significantly increased. Thus, the output power of the analyzed amplifier is lower than the average of commercial Class-D amplifiers.

Finally, the conduction loss-optimized stage showed greater efficiency, since the transistors were dimensioned for this, at the expense of a high area consumption. While in the stage optimized for switching losses, the maximum current required by the load limits the reduction of the output transistors, which establishes a minimum value of switching losses, limiting the efficiency of the stage. However, the reduced area and efficiency far above linear amplifiers make this optimization ideal for low-power applications.

Table II compares the results in conduction optimization obtained with other work in the literature.

TABLE I
COMPARISON OF THE OUTPUT STAGES

	Conduction Losses	**Switching Losses**
W/L PMOS ($\mu m/\mu m$)	27714	6909
W/L NMOS ($\mu m/\mu m$)	8571	2143
Total Area (μm^2)	4445	1109
Average Output Power (mW)	60.9	4.0
Average Efficiency (%)	89.1	74.8

TABLE II
COMPARISON BETWEEN CONDUCTION OPTIMIZATIONS

	This work	**[5]**
Width PMOS (mm)	9.7	12
Width NMOS (mm)	2.4	3
Efficiency (%)	89	97
Output Power (mW)	60.9	49.4
CMOS Node (nm)	350	180
Supply Voltage (V)	3.3	1.8

IV. CONCLUSION

The work in question presented a review of the Class-D amplifier, detailed the design of an amplifier using a commercial CMOS 0.35 μm technology, and compared the performance parameters considering the optimized output stages for two different operating regions.

The result of the simulations shows a high efficiency, if compared with the linear amplifiers. For the output stage optimized for switching losses, we obtained an average efficiency of 74.8%, while the output stage optimized for conduction losses achieved an average efficiency of 89.1%.

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